Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec– 2018**

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| **Code :** | **17CS2003** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course Outcome** | **Marks** |
| 1. | a. | List out the functions of a computer. Draw the top level structure view of a computer and explain each block. | CO2 | 10 |
| b. | Explain the steps involved in instruction execution. Draw Instruction cycle state diagram and explain. | CO2 | 10 |
| (OR) | | | |  |
| 2. | a. | How interrupts are handled in program sequence? Explain with example. | CO3 | 6 |
| b. | A four way set associative cache has lines of 16 bytes and a total size of 8kB. The 16 Mbyte main memory which is byte addressable. Show the format of main memory addresses. | CO6 | 7 |
| c. | Write about fully associative cache organization. | CO6 | 7 |
|  |  |  |  |  |
| 3. | a. | Distinguish between SRAM and DRAM. | CO6 | 5 |
| b. | For the 8 bit word 11000010, the check bits stored with it would be 0010. Suppose when the word is read from memory, the check bits are calculated to be 1001. What is the data word that was read from memory? | CO2 | 7 |
| c. | Write a note on disk physical characteristics and performance parameters. | CO1 | 8 |
| (OR) | | | |  |
| 4. | a. | Explain RAID levels. | CO3 | 10 |
| b. | Explain the functions of 82C55A programmable peripheral interface and DMA controller. | CO1 | 10 |
|  |  |  |  |  |
| 5. | a. | Write one, two and three address instruction code to compute A = ( B\*C) – ( D+E). | CO1 | 10 |
| b. | Explain types of operations with an example for each type. | CO2 | 10 |
| (OR) | | | |  |
| 6. | a. | Explain addressing modes with an example. | CO3 | 10 |
| b. | Write Booth’s Algorithm for Twos Complement Multiplication and explain. | CO2 | 10 |
|  |  |  |  |  |
| 7. | a. | Write Short note on register organization. | CO1 | 5 |
| b. | Explain instruction pipeline operations. | CO4 | 10 |
| c. | How will you optimize the execution of branching statements? | CO4 | 5 |
| (OR) | | | |  |
| 8. | a. | What do you mean by Pipeline Hazards? Explain all types of Hazards. | CO3 | 15 |
| b. | Draw branch prediction state diagram and explain. | CO3 | 5 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Draw block diagram of Intel 8085 and explain . | CO1 | 10 |
| b. | Write micro operations for the following:   1. Instruction Fetch cycle. 2. Fetch source operand. 3. Interrupt cycle. 4. Execute cycle for any one instruction. | CO5 | 10 |